a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation; and

a socket adapted to receive the memory module and to couple the memory module to the unidirectional command and address bus and to the bidirectional data bus.

14. (Amended) The memory system according to claim 13 wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of the memory [subsystem] module and a second delay introduced by the data register of the memory [subsystem] module.

Please add the following new claims:

32. (New) A method of storing data in a pipelined memory system, wherein the pipelined memory system includes a memory module, a socket, and a plurality of memory devices, wherein each memory device includes addressable storage, a data in and a data out buffer, a column decoder, and a row decoder, and wherein the socket couples the memory module to a unidirectional command and address bus and to a bidirectional data bus, the method comprising:

inserting the memory module in the socket;

communicating commands and addresses, through the socket to the memory module, on the unidirectional command and address bus;

communicating data, through the socket to the memory module, on the bidirectional data bus;

latching the commands and addresses in a buffer register;

latching the data in a data register;

driving the latched commands and addresses to the column and row decoders;

driving the latched data to the data in buffers; and

storing the data in the addressable storage of one of the plurality of memory devices.

33. (New) The method of claim 32, wherein communicating commands and addresses and communicating data includes executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

34. (New) A method of reading data in a pipelined memory system, wherein the pipelined memory system includes a memory module and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, the method comprising:

inserting the memory module in the socket;

communicating commands and addresses, through the socket to the memory module, on the unidirectional command and address bus;

latching the commands and addresses in a buffer register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

communicating data from the addressable storage of one of the plurality of memory devices;

latching the data in a data register; and

communicating the data, through the socket to a memory controller, on the bidirectional data bus.

35. (New) The method of claim 34, wherein communicating commands and addresses and receiving data includes executing a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

36. (New) A memory module comprising:

a data register;

a buffer register;

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer, a column decoder and a row decoder, wherein the data in buffer receives data information from the data register and wherein the column decoder and row decoder receive address information from the buffer register; and

a connector, wherein the connector includes command and address lines coupled to the buffer register and data lines coupled to the data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus.

37. (New) The memory module of claim 36, wherein the address information and the data information are communicated according to a packet-protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

38. (New) The memory module of claim 36, wherein each memory device is a dynamic random access memory device.

39. (New) The memory module of claim 36, wherein M equals 8.

40. (New) A method of storing data in a memory module having a connector, wherein the connector includes command and address lines coupled to a buffer register and data lines coupled

to a data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus, the method comprising:

coupling the connector to the socket;

receiving commands and addresses, through the command and address lines, from the unidirectional command and address bus;

receiving data, through the data lines, from the data bus;

latching the commands and addresses in a buffer register;

latching the data in a data register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

driving the latched data to the plurality of memory devices; and

storing the data in the addressable storage of one of the plurality of memory devices.

41. (New) The method of claim 40, wherein the commands and addresses and the data is communicated according to a packet-protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

42. (New) A method of reading data in a memory module having a connector, wherein the connector includes command and address lines coupled to a buffer register and data lines coupled to a data register, wherein the connector is capable of being connected through a socket to a unidirectional command and address bus and a data bus, the method comprising:

coupling the connector to the socket;

receiving commands and addresses, through the command and address lines, from the unidirectional command and address bus;

latching the commands and addresses in a buffer register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

reading data from the addressable storage of one of the plurality of memory devices;

latching the data in a data register; and

communicating the data, through the data lines, to the data bus.

43. (New) The method of claim 42, wherein the commands and addresses and the data is communicated according to a packet-protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

44. (New) An electronic system comprising:

a microprocessor;

a memory controller coupled to the microprocessor;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a memory module, wherein the memory module includes:

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation; and

a socket adapted to receive the memory module and to couple the memory module to the unidirectional command and address bus and to the bidirectional data bus.

45. (New) The electronic system of claim 44, wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of the memory module and a second delay introduced by the data register of the memory module.

46. (New) The electronic system of claim 44, wherein each memory device is a dynamic random access memory device.

47. (New) The electronic system of claim 44, wherein M equals 8.

48. (New) In an electronic system having a memory controller, a memory module, wherein the memory module includes a plurality of memory devices, and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, a method of storing data in one of the plurality of memory devices comprising:

inserting the memory module in the socket;

communicating information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses to the unidirectional command and address bus;

communicating the commands and addresses from the unidirectional command and address bus, through the socket, to the memory module;

communicating data from the memory controller to the bidirectional data bus;

communicating the data from the bidirectional data bus to the memory module;

latching the commands and addresses in a buffer register;

latching the data in a data register;

driving the latched commands and addresses to the plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

driving the latched data to the data in buffers; and

storing the data in the addressable storage of one of the plurality of memory devices.

49. (New) The method of claim 48, wherein communicating commands and addresses and communicating data includes executing a pipeline packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

50. (New) In an electronic system having a memory controller, a memory module, wherein the memory module includes a plurality of memory devices, and a socket, wherein the socket couples the memory module to a unidirectional command and address bus and a bidirectional data bus, a method of reading data from one of the plurality of memory devices comprising:

inserting the memory module in the socket;

communicating information to the memory controller, wherein the memory controller receives the information and wherein the memory controller issues commands and addresses to the unidirectional command and address;

communicating the commands and addresses from the unidirectional command and address bus, through the socket, to the memory module;

latching the commands and addresses in a buffer register;

driving the latched commands and addresses to a plurality of memory devices having addressable storage, wherein each memory device includes a data in and a data out buffer, a column decoder, and a row decoder;

communicating data from the addressable storage of one of the plurality of memory devices;

latching the data in a data register; and

communicating the data, through the socket to the memory controller, on a bidirectional data bus.

51. (New) The method of claim 50, wherein communicating commands and addresses and receiving data includes executing a pipeline packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

52. (New) A memory system, comprising:

a unidirectional command and address bus in electrical communication with a memory control device;

a bidirectional data bus in electrical communication with the memory control device;

a memory module, wherein the memory module includes:

a plurality M of memory devices, wherein each memory device contains a data in and a data out buffer;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching data information from the bidirectional data bus and driving the data information to the data in buffers of the plurality of memory devices for a write operation, the data register receiving and latching the data information from the data out buffers of the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation; and

a socket adapted to receive the memory module and to couple the memory module to the unidirectional command and address bus and to the bidirectional data bus.

53. (New) The memory system of claim 52, wherein the commands and addresses and the data information communicate using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

54. (New) The memory system of claim 52, wherein each memory device is a dynamic random access memory device.

55. (New)The memory system of claim 52, wherein M equals 8.

CONCLUSION

Non-elected claims 1-12 and 17-31 have been canceled without prejudice and not in response to an art rejection. Applicant reserves the right to reintroduce these claims at a later date or in a continuation or divisional patent application. Claims 13 and 14 have not been amended in response to any art rejection. New claims 32-55 are drawn to the control of pipelined memories including the use of a socket adapted to receive a memory module and fit within Group IV of the Restriction Requirement of the parent case.

Claims 13-16 and 32-55 are now pending in this application. The Examiner is invited to contact the below-signed attorney to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

KEVIN J. RYAN

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6904

Date Nov. 5, 1999 By Daniel J. Kluth
Daniel J. Kluth
Reg. No. 32,146

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